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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes

Title: PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Docket No.: 1303.029US1
Filed: August 30, 2001
Examiner:

Serial No.: 09/945,500
Due Date: N/A
Group Art Unit: 2818

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Information Disclosure Statement (1 pg.), Form 1449 (2 pgs.), and copies of 33 cited references.
X A Communication Concerning Co-Pending Applications (2 pgs.).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: _____
Atty: Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 26 day of July, 2002.

Gina M. Uphus
Name

Gina Uphus
Signature

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(GENERAL)

#31 D.DS 10/23/02 C. Moore

S/N 09/945,500 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes	Examiner:	
Serial No.:	09/945,500	Group Art Unit:	2818
Filed:	August 30, 2001	Docket:	1303.029US1
Title:	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS		

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
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Date 7/19/2002 By _____

Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 23 day of July, 2002.

Gina M. Uphus
Name

Gina M. Uphus
Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes	Examiner:	
Serial No.:	09/945,500	Group Art Unit:	2818
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COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

Commissioner for Patents
Washington, D.C. 20231

Applicant would like to bring to the Examiner's attention the following related co-pending application(s) in the above-identified patent application:

Serial No.	Filing Date	Attorney Docket	Title
09/256,643	02/23/1999	00303.324US2	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
09/652,420	08/31/2000	00303.324US3	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
09/691,004	10/18/2000	00303.324US4	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
08/903,453	07/29/1997	00303.378US1	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS
09/258,467	02/26/1999	00303.378US2	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS
09/650,553	08/30/2000	00303.378US3	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS
09/669,281	09/26/2000	00303.405US3	PROGRAMMABLE MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS

09/780,169	02/09/2001	01303.003US1	FLASH MEMORY WITH ULTRATHIN VERTICAL BODY TRANSISTORS
10/152,649	02/09/2001	01303.003US2	FLASH MEMORY WITH ULTRATHIN VERTICAL BODY TRANSISTORS
09/945,507	08/30/2001	01303.014US1	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully submitted,

LEONARD FORBES

By Applicant's Representatives,

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Date 7/19/2002 By _____
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Gina M. Uphus
Name

Gina Uphus
Signature